

Thermal-to-high-energy neutron SEU characterization of commercial SRAMs

Andrea Coronetti, Rubén García Alía, Manon Letiche, Carlo Cazzaniga, Maria Kastriotou, Matteo Cecchetto, Kacper Bilko, and Pedro Martín-Holgado

Abstract—Several commercial SRAMs have been tested by the CERN R2E project with neutrons of various energy. The test data are used to cross-compare facilities and to analyze variabilities within SRAMs from the same manufacturer. FIT for atmospheric and ground applications are provided as well as predictions for accelerator soft error rates.

Index Terms—Thermal neutrons, intermediate-energy neutron, spallation neutrons, SRAMs, SEU, facilities, accelerator, atmospheric, ground.

I. INTRODUCTION

Neutrons from thermal- (meV) to high-energy (GeV) are the main contributor to single-event effects (SEE) in the CERN accelerator environment and the main radiation-related threat when it comes to ensuring the required stable beam availability of the Large Hadron Collider (LHC) [1]. In this context, the Radiation to Electronics (R2E) project has conducted a wider investigation on several commercial Static Random Access Memories (SRAM) from various manufacturers on technologies varying from 40 to 130 nm. The analysis was made to quantify the susceptibility of state-of-the-art technology to thermal neutron single-event upsets (SEU) as opposed to the typical high-energy neutron response. To this end, the SRAMs have been characterized in thermal neutron beams, in an Am-Be source at CERN (providing intermediate energy neutron in the 1-10 MeV range) and at the atmospheric-like neutron spallation facility ChipIrr.

In addition to the pure SRAM characterization the activity involved the cross-comparison of the thermal neutron beams available at new installation at the Institute Laue Langevin (ILL), in France, and at the Rutherford Appleton Laboratory (RAL), in the UK, with respect to the standard installation at ILL that CERN has used during the last five years and that is going to be dismissed for radiation to electronics purposes.

This study has received funding from the European Union's Horizon 2020 research and innovation programme under the MSC grant agreement no. 721624 and from the French national program "Investissements d'Avenir, IRT Naoelec", ANR-10-AIRT-05.

Andrea Coronetti (andrea.coronetti@cern.ch) is with CERN, CH-1211 Geneva 23, Switzerland, and with the Department of Physics, University of Jyväskylä, 40014 Jyväskylä, Finland.

Rubén García Alía, Matteo Cecchetto and Kacper Bilko are with CERN, CH-1211 Geneva 23, Switzerland.

Manon Letiche is with Institute Laue Langevin, 71 Avenue des Martyrs, 38000 Grenoble, France.

Carlo Cazzaniga and Maria Kastriotou are with Science and Technology Facilities Council, OX11 0QX Didcot, UK.

Pedro Martín-Holgado are with Centro Nacional de Aceleradores, 41092 Seville, Spain.

II. DEVICES

The list of tested devices is presented through Table I. The smallest technological nodes are available from ISSI and Cypress, whereas Renesas and Alliance are manufactured using larger processes. All the memories are manufactured in identical TSOP-48 pins packages. Note that the Cypress nicknamed CY65E and CY65C come with embedded error correction code (ECC). Thanks to a non-disclosure agreement (NDA) with the manufacturer, it was possible to disable the ECC. Thus, the data here reported refer to the SRAMs with disabled ECC. The reason behind this choice is that it allows better investigating the non-corrected sensitivity of the SRAM and it also enables its use as a radiation monitor for the LHC accelerator chain [2]. All the SRAMs were tested at nominal 3.3 V I/O voltage and at room temperature.

III. EXPERIMENTS

This section shortly describes the test procedure and the facilities used to irradiate the SRAMs.

The test setup consists of a Field-Programmable Gate Array (FPGA)-based memory tester that performs write and read operations on the memory and disables the ECC when needed. Each memory was written with a checkerboard pattern, the beam was turned on and the memory was continuously read during irradiation and until the beam was turned off. The readout frequency depended on the beam flux available at the facility, but it was always in the range of 5-60 seconds. Whenever errors were found and logged, the corresponding address was rewritten to the correct checkerboard pattern.

A. ILL - D50

D50 [3], [4] is the former installation at ILL used for irradiation to electronics that will no longer be used for such purpose as of 2021. The fast neutrons released by the reactor are cooled down to thermal energies (peaking at 13 meV) by means of liquid deuterium at 20 K. The corresponding equivalent thermal neutron flux (at 25 meV) was 1.1×10^9 n/cm²/s at the time of these tests.

B. ILL - TENIS

TENIS is the current and future installation at ILL for irradiation of electronics. The neutrons available at the device under test (DUT) are mainly thermal neutrons, but there is an epithermal and intermediate energy tail typical of fission reactor spectra. Through gold foil activation the 25 meV equivalent

TABLE I
LIST OF TESTED DEVICES.

Nickname	Reference	Manufacturer	Technology [nm]	Array size [Mbit]	Datecode	Embedded ECC
IS40-32	IS61WV204816BLL-10TLI	ISSI	40	32	2020	No
IS40-16	IS61WV102416BLL-10TLI	ISSI	40	16	2004	No
IS65	IS62WV102416DBLL-45TLI	ISSI	65	16	1834	No
RM110	RMLV0816BGSA-4S2	Renesas	110	8	9062	No
AS90	AS6C3216A-55TIN	Alliance	90	32	2002	No
CY65E	CY62167GE30-45ZXI	Cypress	65	16	1919	Yes
CY65NA	CY62167GN30-45ZXI	Cypress	65	16	1731	No
CY65NB	CY62167G30-45ZXI	Cypress	65	16	1601	No
CY65C	CY7C1061GE30-10ZXI	Cypress	65	16	1649	Yes
CY90	CY62167EV30LL-45ZXA	Cypress	90	16	1843	No
CY130	CY62167DV30LL-55ZXI	Cypress	130	16	1725	No

thermal neutron flux was determined as 2.8×10^9 n/cm²/s at the time of the tests. Similarly to D50 the flux is continuous and uniform over a surface of about 2 cm diameter. Part of the SRAM experiments were performed to characterize the contribution of the intermediate and high energy neutrons (that are negligible in D50) on the overall retrieved SEU cross-section in this new beamline.

C. RAL - EMMA

EMMA [5] is a thermal neutron irradiation installation built around the synchrotron target station 1 at the RAL complex. Differently from ILL, the thermal neutrons are obtained from the spallation of high-energy protons (800 MeV) with a tungsten target and also cooled down to thermal energies by means of moderators. The thermal neutrons are produced according to the synchrotron frequency, which is set to 40 Hz for the target station 1. The equivalent thermal neutron flux is about 1.42×10^6 n/cm²/s and measured with a gas electron multiplier. Similarly to TENIS, the beam can contain not only thermal neutrons, but also epithermal neutrons. The beam is uniform on 4x4 cm² surface.

D. CERN - Am-Be source

The Am-Be source available at CERN [6] provides a continuous spectrum of neutrons up to about 10 MeV, without a significant contribution from thermal neutrons and peaking at 3 MeV. The activity of the source allows reaching a high-energy hadron equivalent flux [7] of 1.84×10^4 n/cm²/s at a distance of 5 cm from the center of the source. The neutron spectrum is emitted isotropically from the source and the surface homogeneity ($\pm 10\%$) at 5 cm from the source is guaranteed over a surface with 1.5 cm diameter.

E. RAL - ChipIr

The ChipIr [8], [9] irradiation installation at RAL provides atmospheric-like high-energy neutrons from spallation of 800 MeV neutrons with a tungsten target at the target station 2. In this case the beam is pulsed at 10 Hz (and it is actually made of 2 bunches of the duration of 70 ns separated 360 ns apart). The fast neutrons provide an acceleration factor of about 10^9 with respect to the sea level neutron fluxes. The flux above 10 MeV can be as high as $5 \cdot 10^6$ n/cm²/s and,

for these tests, it was made homogeneous over a 7x7 cm² area, although larger areas are possible. The thermal neutron component of the beam is negligible. Thanks to the strong penetration of the beam, it is possible to stack several devices one after the other with no large variations in terms of flux.

IV. DATA ANALYSIS

The data are presented with error bars calculated at 95% confidence level considering the uncertainty on the fluence ($\pm 10\%$) and on the number of events. In those cases for which zero or just a few events were observed the upper bound on the cross-section is reported. The latter is calculated with 95% confidence according to Poisson statistics [10]. All measurements with B₄C, used to filter out the thermal and epithermal neutrons and deduce the fast neutron component of the beam, were performed by placing a 4 mm equivalent B₄C slab in front of the DUT. Note that in this case, the flux after the B₄C was not measured and the cross-sections are computed by means of the unfiltered flux.

A. Cross-comparison of thermal neutron facilities

Table II reports the single-bit upset (SBU) cross-sections measured at the three different thermal neutron irradiation facilities. All the chips that were tested at TENIS with unfiltered beam were also tested with B₄C shielding.

Due to the relatively low flux, only three chips were tested at EMMA. When using the B₄C shielding at both D50 and EMMA 0 events were always measured for all the chips, showing that the SEU contribution from intermediate- and high-energy neutrons at this facilities is completely negligible. A small amount of events (yielding the very large error bars) was measured at TENIS with the same B₄C shielding employed at D50 and EMMA. This demonstrates that there is a small residual component of intermediate-energy neutrons within the TENIS beam. The ratio between the SEU rates for the unfiltered and the filtered spectra is larger than 100 for all the tested chips. It can thus be considered that the intermediate-energy part will contribute for $< 1\%$ to the total SEU count, which is an acceptable uncertainty on the thermal neutron cross-sections.

When considering the unfiltered thermal neutron spectra, slightly higher cross-sections were measured at TENIS than D50, and some of them are very compatible with the

TABLE II
THERMAL NEUTRON SBU CROSS-SECTIONS OF THE VARIOUS DEVICES IN UNITS OF cm^2/BIT .

Nickname	D50	TENIS	TENIS (B ₄ C)	EMMA
IS40-32	$(3.16 \pm 0.64) \times 10^{-15}$	$(3.53 \pm 0.71) \times 10^{-15}$	$(7.45 \pm 4.80) \times 10^{-18}$	$(2.69 \times \pm 0.66) \times 10^{-15}$
IS40-16	$(6.43 \pm 1.40) \times 10^{-16}$	-	-	-
IS65	$(1.02 \pm 0.22) \times 10^{-15}$	$(1.06 \pm 0.23) \times 10^{-15}$	$(7.81 \pm 6.80) \times 10^{-18}$	-
RM110	$< 6.68 \times 10^{-18}$	$< 2.63 \times 10^{-18}$	$< 2.63 \times 10^{-18}$	-
AS90	$(1.42 \pm 0.29) \times 10^{-15}$	$(1.63 \pm 0.23) \times 10^{-15}$	$(8.51 \pm 5.2) \times 10^{-18}$	-
CY65E	$(4.91 \pm 1.10) \times 10^{-16}$	$(6.24 \pm 1.40) \times 10^{-16}$	$(6.39 \pm 6.20) \times 10^{-18}$	$(4.98 \pm 1.20) \times 10^{-16}$
CY65NA	$< 7.95 \times 10^{-18}$	-	-	-
CY65NB	$(5.17 \pm 1.10) \times 10^{-16}$	-	-	-
CY90	$(3.88 \pm 0.92) \times 10^{-16}$	-	-	$(3.33 \pm 0.98) \times 10^{-16}$
CY130	$(2.49 \pm 0.58) \times 10^{-16}$	-	-	-

intermediate-energy contamination previously mentioned. The maximum discrepancy, observed for CY65E, was less than 20%. This same chip is the one providing the best cross-comparison between D50 and EMMA. For the other two chips, slightly lower cross-sections were measured at EMMA, with a difference of less than 15%. Hence, it can be concluded that SEU cross section differences between the same components and diverse thermal neutron beams were below 20% and, therefore, compatible with typical experimental uncertainties.

The memory IS40-32 is the only one for which multiple-bit upsets (MBU) were observed with thermal neutrons. Less than 1 in 200 events were MBUs when testing in TENIS, whereas this ratio has further reduced to less than 1 in 1000 when testing in D50. No MBUs were measured at EMMA on this memory, but overall upset statistics were lower.

B. Thermal-to-high energy neutron responses

Table III reports the intermediate-energy neutron SBU cross-sections measured with the Am-Be source at CERN and the high-energy neutron SBU cross-sections measured at ChipIr. Note that the fluence used for the Am-Be source is the high-energy hadron equivalent, which is calculated according to the intermediate-energy SEU cross-section of the Toshiba 400 nm SRAM [7], which may more or less be adapted depending on the single memory [6].

The RM110 SRAM performed very well in all the neutron environments from thermal-to-high energy. A bunch of SBUs were actually only observed during the ChipIr test, while all other upper bounds were calculated upon 0 events. The hardness of this memory is due to the presence of DRAM capacitors that increase the critical charge, as it was also observed in previous chips from Renesas [11]. This makes it a promising SRAM to be employed in equipment for neutron-dominated environments.

For the AS90 it was possible to perform standard SBU characterization only with thermal neutrons. For intermediate-energy neutrons the memory suffered from localized row/column SEFIs (MBUs, errors in the same word, in amount as large as SBUs were detected). These SEFIs could not be separated from SBUs, thus the very high cross-section. Due to these problems, the chip was not scheduled for testing at ChipIr because it is not deemed adapt for radiation tolerant

equipment as well as for radiation monitoring purposes that require read-write operations to be performed under radiation.

The CY90 and CY130 chips had very similar cross-sections for thermal and intermediate-energy neutrons. However, the measurements in the atmospheric-like spectrum at ChipIr for the CY130 SRAM were inconclusive. Two different units were probed and both of them, at some point during irradiation, returned errors over the full memory array. This seems to be an indication of single-event latchup (SEL), although the test setup was not meant to detect such event and this cannot be confirmed at this time. For both SRAMs such events were detected for fluences lower than $3 \times 10^9 \text{ n/cm}^2$.

Concerning the various Cypress SRAMs based on 65 nm technology, CY65E, CY65NA and CY65NB are electrically equivalent, but, apparently, only CY65E and CY65NB are equivalent in terms of radiation response all over the considered energy range for testing. Two units of CY65NA were tested with thermal neutrons to the same fluence as their CY65E and CY65NB counterparts, but they showed only 2-3 events (instead of several hundreds). CY65NA has, however, the same intermediate and high-energy neutron cross-section of CY65E and CY65NB.

These observations implies that their radiation response differs only for thermal energies. Variations in the thermal neutron energies can only come from the different boron implantations. This suggests that CY65NA is manufactured according to a different process than CY65E and CY65NB. This is interesting since CY65NA and CY65NB have almost identical intermediate- and high-energy neutron cross-section, hence, they could be used to obtain a differential measurement of thermal neutron fluxes for radiation environments typical of accelerators and nuclear reactors.

The CY65C SRAM is not electrically equivalent to the other three. For this memory the fastest access time is downsided by a higher power consumption. Although the SRAM was not tested with thermal neutrons (no ECC disabling available at the time of the test for this chip), the intermediate- and high-energy neutron SBU cross-sections are about 60% less than the other three chips manufactured in 65 nm technology.

The variability for the three SRAMs manufactured by ISSI is more pronounced and it is further stressed in Figure 1. Even though IS40-16 and IS40-32 are supposed to be the

TABLE III
INTERMEDIATE- AND HIGH-ENERGY NEUTRON SBU CROSS-SECTIONS OF
THE VARIOUS DEVICES IN UNITS OF cm^2/BIT .

Nickname	Am-Be	ChipIr
IS40-32	$(2.88 \pm 0.63) \times 10^{-14}$	$(9.69 \pm 2.00) \times 10^{-15}$
IS40-16	$(5.48 \pm 1.50) \times 10^{-14}$	$(3.86 \pm 0.85) \times 10^{-14}$
IS65	$(6.36 \pm 1.70) \times 10^{-14}$	$(7.41 \pm 1.60) \times 10^{-14}$
RM110	$< 4.73 \times 10^{-16}$	$< 7.82 \times 10^{-18}$
AS90	$(1.21 \pm 0.24) \times 10^{-12}$	-
CY65E	$(1.25 \pm 0.26) \times 10^{-13}$	$(1.16 \pm 0.24) \times 10^{-13}$
CY65NA	$(1.33 \pm 0.29) \times 10^{-13}$	$(1.22 \pm 0.26) \times 10^{-13}$
CY65NB	$(1.31 \pm 0.30) \times 10^{-13}$	$(1.11 \pm 0.23) \times 10^{-13}$
CY65C	$(5.02 \pm 1.30) \times 10^{-14}$	$(4.97 \pm 1.10) \times 10^{-14}$
CY90	$(5.09 \pm 1.10) \times 10^{-14}$	$(3.95 \pm 0.80) \times 10^{-14}$
CY130	$(4.87 \pm 1.20) \times 10^{-14}$	(*)

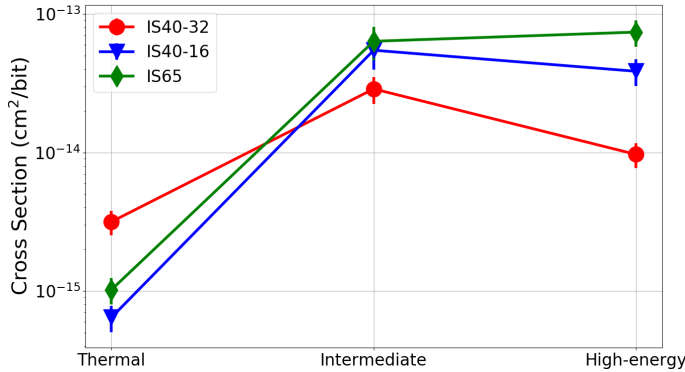


Fig. 1. Thermal-, intermediate- and high-energy neutron cross-sections of SRAMs manufactured by ISSI.

same memory, with the latter having twice larger array than the former, their radiation response are very different when varying the neutron energy.

IS40-32 has a thermal neutron cross-section a factor of 5 higher than IS40-16. At the same time, it has both lower intermediate- and high-energy neutron cross-sections, by a factor of 2 and of 4, respectively. Apart from pointing out crucial differences in the manufacturing processes, it is expected that the relative thermal neutron contribution to the soft error rate (or the failures in time, FIT) will be drastically different for two chips procured from the same manufacturer and having, to the user's knowledge, only an array size difference.

Although manufactured in a larger technology, IS65 has a much more similar radiation response when varying the neutron energy to IS40-16 than the two identical technology nodes do. More or less a factor 2 higher cross-section is observed for IS65 from thermal-to-high-energy over IS40-16, pointing out slight improvements in SBU response when shrinking the technology.

C. Intra-lot variability

An intra-lot SEU cross-section variability analysis was performed over the IS40-32 and CY65E. The D50 facility was used for the purpose and 20 samples from the reported lot of

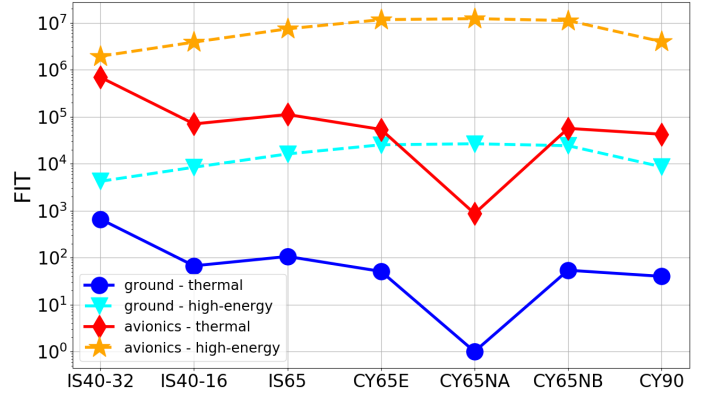


Fig. 2. FITs for ground and avionics (12 km altitude) from thermal and high-energy neutrons for the tested devices.

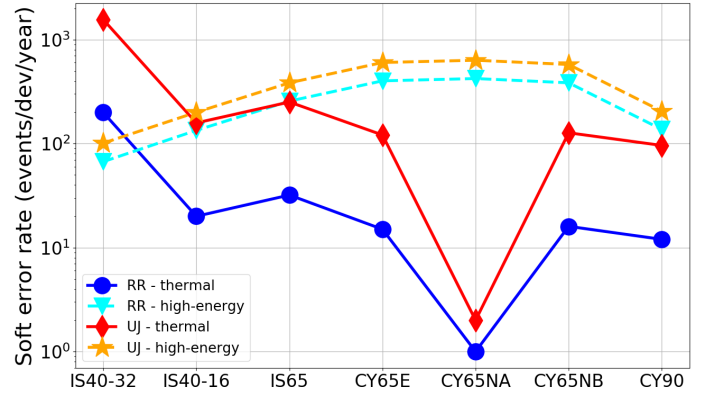


Fig. 3. Soft error rates for lightly (RR) and heavily (UJ) shielded alcoves at CERN from thermal and high-energy neutrons for the tested devices. Environmental data are based on the position RR13 and UJ16 following RadMon measurements of the thermal and high-energy hadron fluxes during the 2018 LHC run [12].

IS40-32 were irradiated and 16 samples from the reported lot for the CY65E.

In summary, it was found that the average SEU cross-section over the 20 samples of the IS40-32 was $3.17 \times 10^{-15} \text{ cm}^2/\text{bit}$. The 2σ intra-lot variability with respect to the average was found to be $\pm 2.57 \times 10^{-16} \text{ cm}^2/\text{bit}$, i.e., $\pm 8.1\%$.

For the CY65E the average SEU cross-section over the 16 samples was $4.76 \times 10^{-16} \text{ cm}^2/\text{bit}$. The 2σ intra-lot variability with respect to the average was found to be $\pm 7.75 \times 10^{-17} \text{ cm}^2/\text{bit}$, i.e., $\pm 16.2\%$.

Therefore, the IS40-32 SRAM is not only more sensitive to thermal neutrons, but it guarantees a better accuracy for measurements of thermal neutron fluxes in new facilities or in accelerator mixed-field.

D. Soft error rates

Fig. 2 reports the failures in time (FIT) due to thermal and high-energy neutrons for the devices for which both cross-sections are available. The data are shown for ground and avionics applications (12 km altitude).

For most of the devices, the FIT is still dominated by fast neutrons, with thermal neutrons contributing for as low as 1%. Only the device IS40-32 is expected to have a sizeable

impact from thermal neutrons of 13% and 26% for ground and avionics, respectively.

Fig. 3 reports the soft error rate in units of events/device/year expected in lightly (RR) and heavily shielded (UJ) [12] alcoves for electronic equipment at the CERN LHC.

Thermal neutrons are expected to provide a non-negligible contribution to all the ISSI devices (even dominant for IS40-32, even more than 90% for UJ, see also [12]), whereas the contribution for Cypress devices is lower (typically below 30% for UJ).

V. ACKNOWLEDGMENTS

We recognize the contribution of Helmut Puchner from Cypress Semiconductors for disclosing the information required to disable the embedded ECC in the CY65E and CY65C SRAMs.

REFERENCES

- [1] R. García Alía et al., "Single event effects in high-energy accelerators," *Semicond. Sci. Technol.*, vol. 32, no. 0340003, Feb. 2017.
- [2] G. Spiezia et al., "A new RadMon version for the LHC and its injection lines," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3424-3431, Dec. 2014.
- [3] A. Coronetti et al., "SEU characterization of commercial and custom-developed SRAMs based on 90 nm technology and below," *Radiation Effects Data Workshop Rec.*, Dec. 2020.
- [4] M. Cecchetto et al., "Impact of thermal and intermediate energy neutrons on the semiconductor memories for the CERN accelerators," *M.S. Thesis*, Dept. Inf. Eng., Padova Univ., Padua, Italy, 2017.
- [5] C. Cazzaniga, D. Raspino, G.J. Sykora, and C.D. Frost, "Dosimetry of thermal neutron beamlines at a pulsed spallation source for the application to the irradiation of microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 921-927, May 2021.
- [6] M. Cecchetto et al., "0.1-10 MeV Neutron Soft Error Rate in Accelerator and Atmospheric Environments," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 873-883, May 2021.
- [7] K. Roed et al., "Method for measuring mixed field radiation levels relevant for SEEs at the LHC," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 1040-1047, August 2012.
- [8] C. Cazzaniga, M. Bagatin, S. Gerardin, A. Costantino, C.D. Frost, "First tests of a new facility for device-level, board-level and system-level neutron irradiation of microelectronics," *IEEE Trans. Emerg. Topics Comput.*, vol. 9, no. 1, pp. 104-108, Jan. 2021.
- [9] D. Chiesa, M. Nastasi, C. Cazzaniga, M. Rebai, L. Arcidiacono et al., "Measurement of the neutron flux at spallation sources using multi-foil activation," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 902, pp. 14-24, Sept. 2018.
- [10] G.M. Swift, "SEE testing lessons from Dickens, Scouting and Oz," *SEE Symposium*, Logan, UT, USA, 2006.
- [11] S. Uznanski et al., "The Effect of Proton Energy on SEU Cross Section of a 16Mbit TFT PMOS SRAM with DRAM Capacitors," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3074-3079, Dec. 2014.
- [12] M. Cecchetto et al., "Thermal neutron-induced SEUs in the LHC accelerator environment," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1412-1420, July 2020.